Low Power Ultra Long Range Transceiver

General Description

The WA1470 is a high-performance low power RF transceiver intended for RF wireless applications in the sub-1 GHz band.

The WA1470 transceiver operates in the 430 - 500 MHz and 860 - 925 MHz frequency ranges.

The WA1470 transceiver supports high performance NB-Fi protocol with data rates 50 - 25 600 bit/s, with exceptional receiving sensitivity down to -148 dBm.

Operation for WA1470 transceiver is specified over the industrial temperature range, from -40°C to 85°C.

Applications

- Smart Metering
- Smart lighting systems
- Wireless alarm and security systems
- Industrial monitoring and control
- Wireless sensor networks
- Smart Agriculture
- IoT low data rate wireless applications

Key Product Features

High sensitivity/High selectivity Receiver:

- NB-Fi MAC level compliance
- Data rates: 50, 100, 400, 3200, 25600 bps
- Sensitivity:
  - -148 dBm @ 50 bps, 868 MHz
  - -145 dBm @ 100 bps, 868 MHz, Frequency Hopping mode
  - -139 dBm @ 400 bps, 868 MHz
  - -130 dBm @ 3200 bps, 868 MHz
  - -121 dBm @ 25600 bps, 868 MHz
- Adjacent channel suppression: 80 dB
- Immunity to reference oscillator error up to ±1 ppm for 50 bps receiving

Transmitter:

- Built-in DBPSK modulation with Frequency Hopping support
- Data rates:
  - up to 25 600 bps for NB-Fi packets
  - up to 100 kbps for DBPSK messages
- High Efficiency Power Amplifier
- Maximum Output Power: 15 dBm @ 3.3 V, 868 MHz
- Programmable Power Output Level with < 3 dB step
- Auxiliary input for unmodulated data

- Frequency bands:
  - 430 MHz - 500 MHz
  - 860 MHz - 925 MHz
- Programmable RF Carrier Frequency with 1 Hz step
- Maximum bandwidth: 200kHz

- 4-Wire SPI interface

- Supply voltage range: 1.8 V - 3.6 V
- Low power consumption:
  Rx Mode, from 3.3 V supply:
  - 17 mA @ Low-current LNA mode
  - 23 mA @ Low-NF LNA mode

  Tx Mode, from 3.3 V supply:
  - 50 mA @ 15 dBm
  - 20 mA @ 8 dBm

- QFN32 5x5 mm Package

- Operating temperature range: from -40°C to +85°C

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Block Diagram & Chip Architecture

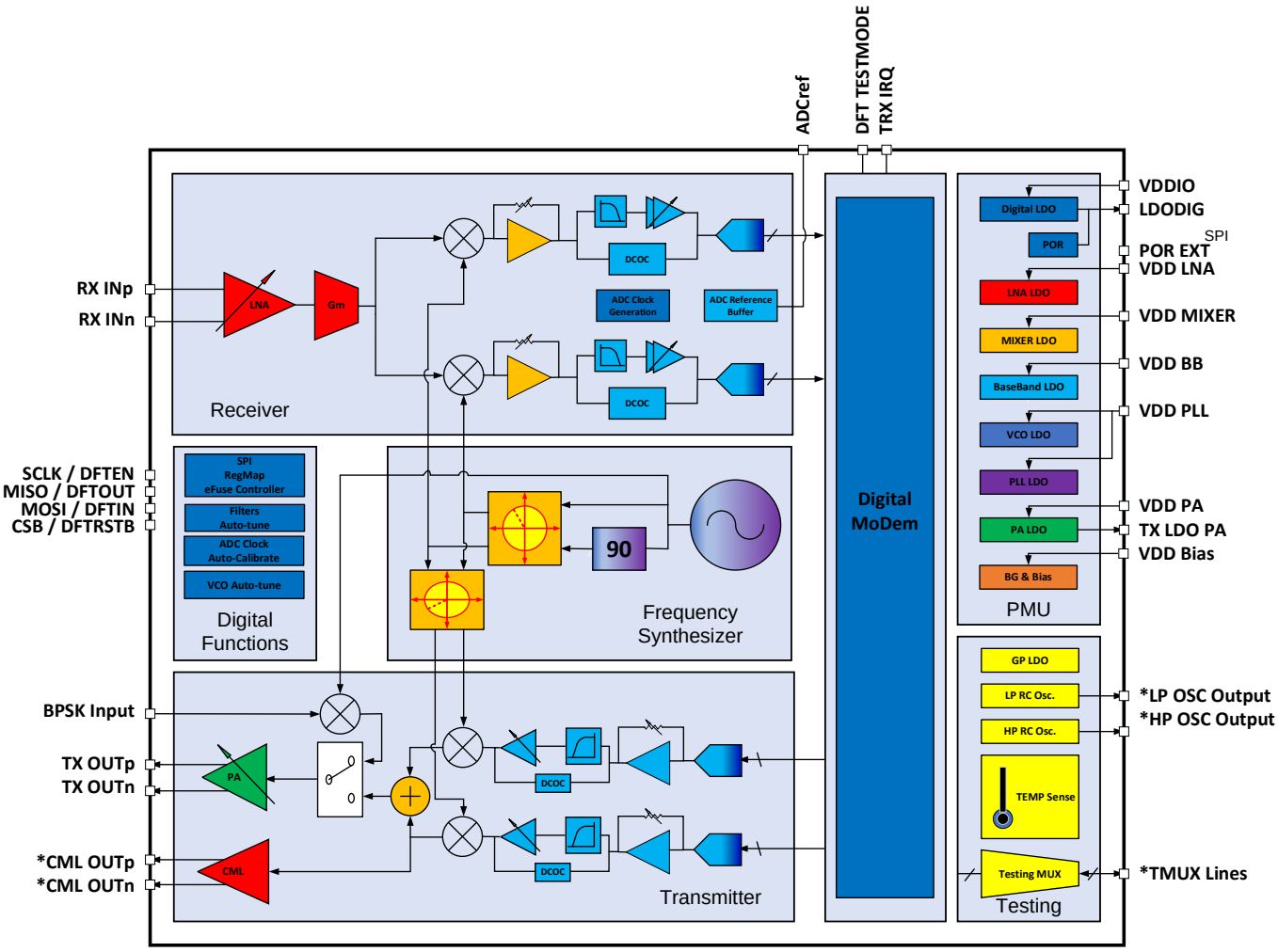


Figure 1: WA1470 Functional Block Diagram

The WA1470 receiver architecture is direct conversion where the received RF signal is converted directly to baseband. The received RF signal is amplified at the input by a differential low noise amplifier (LNA) followed by a trans-conductance (Gm) stage and quadrature down conversion mixer (I and Q) to baseband signal. The baseband signal is amplified and low pass filtered by 4th order active low pass filter (Rx-BB). The output signal from Rx-BB is digitized by analog to digital converter (ADC) and passed to the baseband modem for further processing.

The WA1470 transmitter utilizes direct conversion from baseband digital to analog converter (DAC), followed by an active low pass filter with programmable attenuation to RF frequency and finally output power is generated using an integrated class-E power amplifier (PA). Output power level can be configured from -8 dBm to +15 dBm at antenna with steps of 3 dB as maximum. Input of transmitter DAC is generated by the baseband modem.

The integrated PA is used for constant envelope modulation schemes as BPSK/DPSK. The integrated PA input has two modes:

1. RF input is generated from integrated frequency synthesizer and its phase is modulated by a serial digital data stream (0° and 180°).
2. DAC baseband output is up converted directly to RF frequency in a quadrature architecture (I and Q), then summed up at the PA pre-driver input (Tx mixer output).

In case that a linear PA is required (due to a variable amplitude modulation scheme) or a higher output power level is required, there is a linear CML driver following the Tx mixer to drive an external PA while the integrated (internal) PA will be off in this mode.

The WA1470 has a single input clock for proper operation, TCXO at 26 MHz is expected.

The WA1470 can operate using a voltage supply ranging from 1.8V to 3.6V, based on integrated power management regulators.

A standard 4-pin SPI interface is used to communicate with the external MCU.

One-time programmable memory is integrated to store the ID and some required production trimming controls.

Pin Diagram

The following diagram shows the pin arrangement of the QFN package, top view.

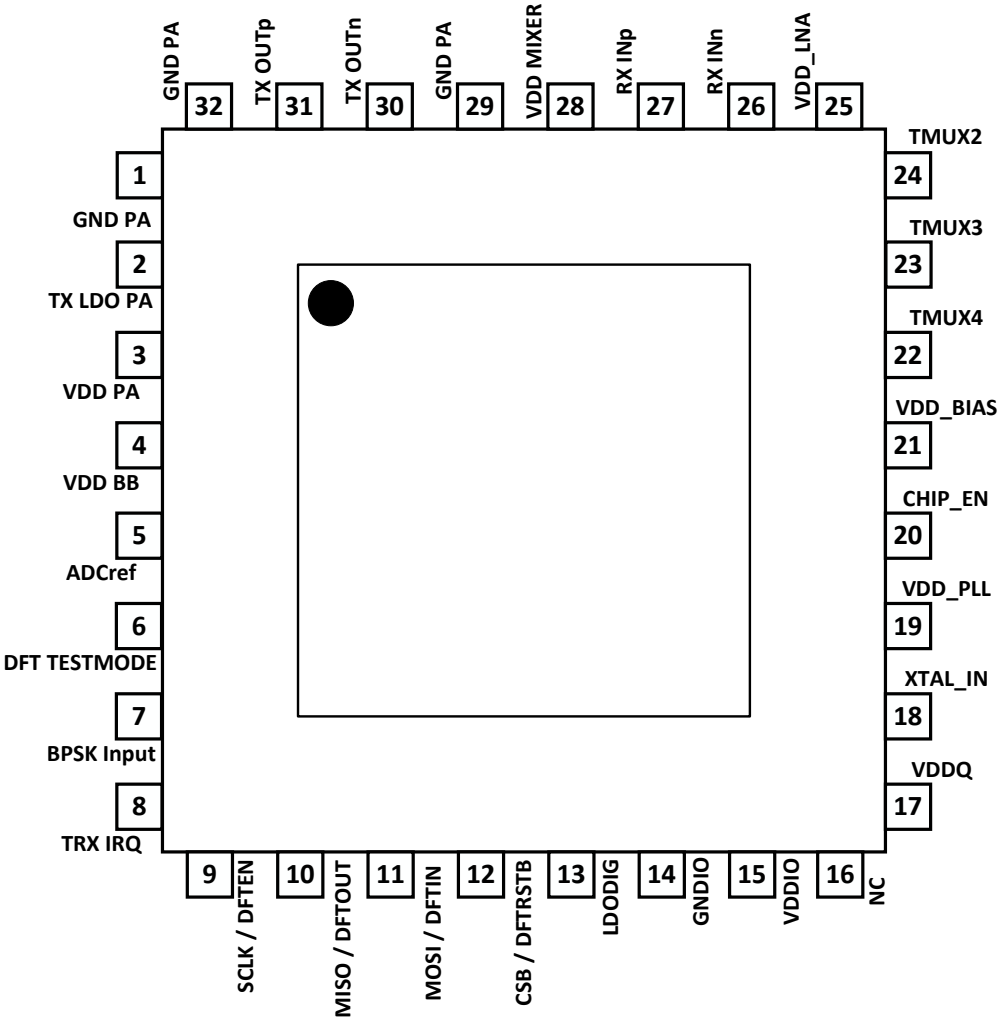


Figure 2: PIN Diagram

Pin List & Description

Table 1: PIN Description

Pin	Pin Name	Description
1	GND_PA	PA ESD Ground
2	TX_LDO_PA	PA LDO output
3	VDD3P3V_PA	PA ESD Supply
4	VDD3P3V_BB	Base-Band ESD Supply

Pin	Pin Name	Description
5	ADCREF	SAR ADC Reference Voltage
6	DFT_TESTMODE	DFT Test Mode Enable
7	BPSK_DATAIN	BPSK Input data
8	TRX_IRQ	Interrupt signal
9	SCLK_DFTEN	SPI clock
10	MISO_DFTOUT	SPI Data Out
11	MOSI_DFTIN	SPI Data In
12	CSB_DFTRSTB	Slave Select
13	LDODIG_1P1V	Digital LDO (1.1 V) output
14	GND_IO	I/O ESD Ground
15	VDD3P3V_IO	I/O ESD Supply
16	NC	Not Connected
17	VDDQ	EFUSE Supply
18	XTAL_IN	Crystal Oscillator Input
19	VDD3P3V_PLL	PLL ESD Supply
20	CHIP_EN	Chip Enable
21	VDD3P3V_BIAS	Bias ESD Supply
22	TMUX4	TMUX line #4
23	TMUX3	TMUX line #3
24	TMUX2	TMUX line #2
25	VDD3P3V_LNA	LNA & Mixers ESD Supply
26	RX_INN	LNA Input
27	RX_INP	LNA Input
28	VDD3P3V_MIXER	Mixers Supply
29	GND_PA	PA ESD Ground
30	TX_OUTN	PA Output
31	TX_OUTP	PA Output
32	GND_PA	PA ESD Ground

Typical Connectivity

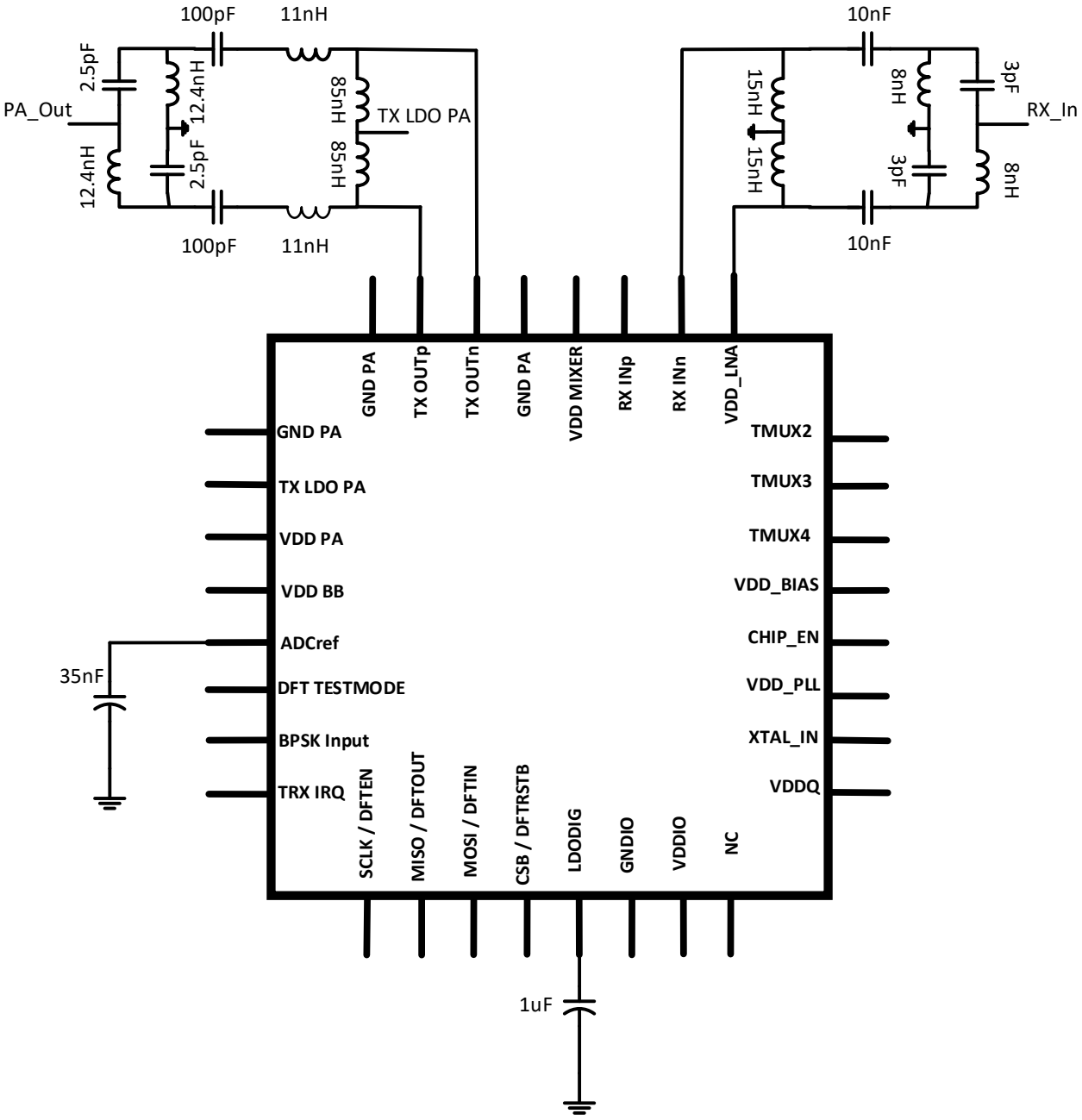


Figure 3: Typical Connectivity @ 860-925 MHz Band

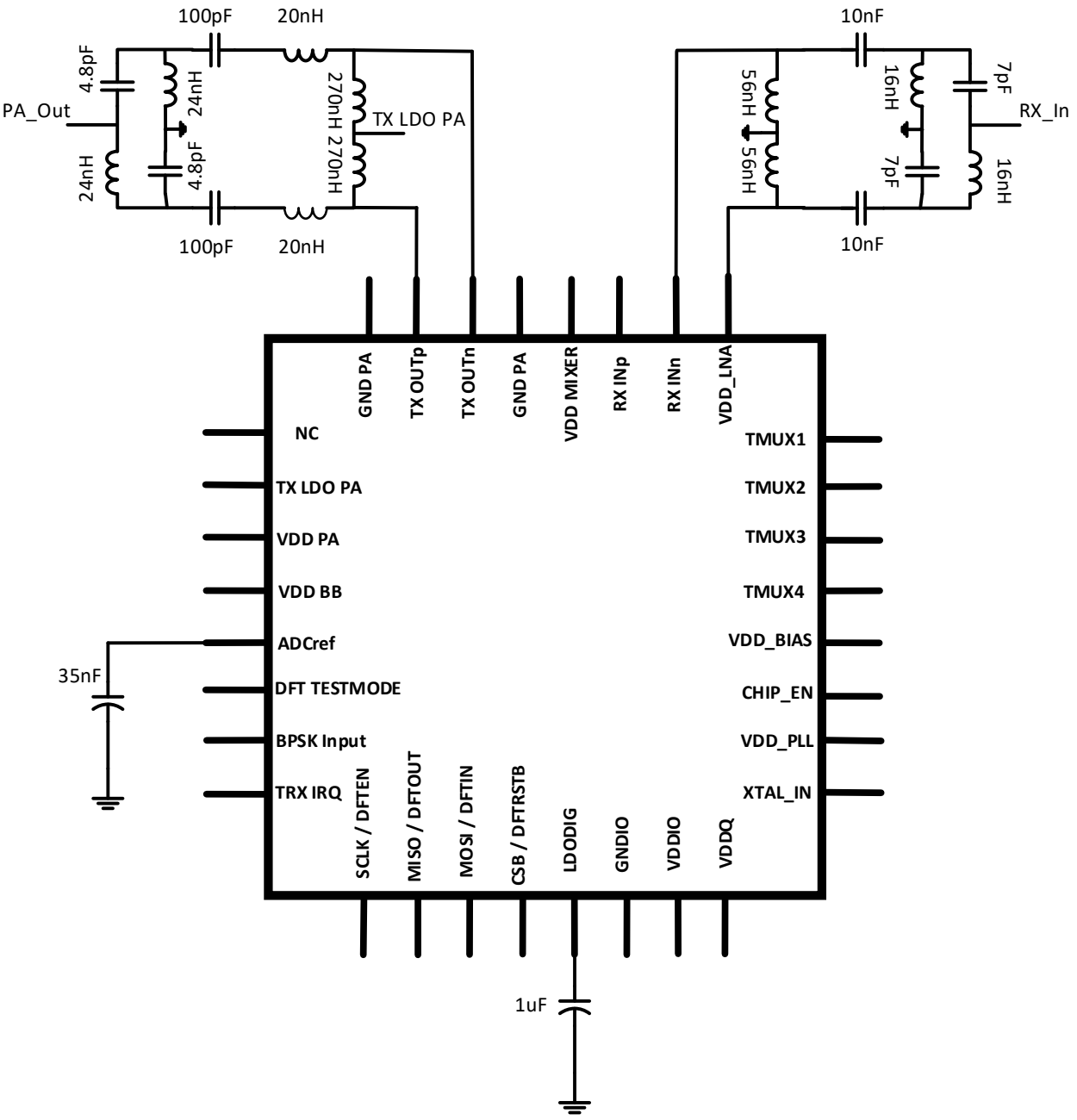


Figure 4: Typical Connectivity @ 430-500 MHz Band

Chip Modes

The transceiver has different modes of operation with different expected transition times and different blocks ON/OFF as indicated in the table 2.

Table 2: Chip Operation Modes and Expected Transition Times

Initial Mode	Initial Mode Conditions	Idle	Normal Rx	Normal Tx	Sleep	Deep Sleep
Idle	All bias circuits are ON All Rx Blocks are OFF All Tx Blocks are OFF LO is ON	N/A	20 us	20 us	20 us	1 ms
Normal Rx	All bias circuits are ON All Rx Blocks are ON All Tx Blocks are OFF LO is ON	10 us	N/A	10 us	20 us	1 ms
Normal Tx	All bias circuits are ON All Rx Blocks are OFF All Tx Blocks are ON LO is ON	10 us	10 us	N/A	20 us	1 ms
Sleep	All bias circuits are ON All Rx Blocks are OFF All Tx Blocks are OFF LO is OFF	3 ms	3 ms	3 ms	N/A	1 ms
Deep Sleep	Core bias circuits[1] are OFF All Rx Blocks are OFF All Tx Blocks are OFF LO is OFF	3 ms	3 ms	3 ms	3 ms	N/A
Shutdown	All circuits are OFF (Analog & Digital)	Transition from shutdown to any other mode is expected in 3ms				

[1] Core bias circuits include reference voltage (bandgap), LDOs (Other than digital LDO) and bias voltage & current for any block other than Rx, Tx & Synthesizer (LO) blocks.

The shutdown mode is not controlled by SPI, it is controlled by a master enable pin.

All other modes (other than shutdown) are controlled by SPI commands where all transitions are allowed as indicated in table 3.

Table 3: Mode controls in different modes of operation

Mode / Control	**TxRx_poff REG47[7]**	**TxRx_sleep REG47[6]**	**TxRx_idle REG47[5]**	**TxON_RxOFF REG47[4]**
Deep Sleep	1	X	X	X
Sleep	0	1	X	X
Idle	0	0	1	X
Normal Tx	0	0	0	1
Normal Rx	0	0	0	0

Specifications

All typical values are at ambient room temperature (25°C) and at supply of 3.3 V.

ESD Ratings

Table 4: WA1470 ESD Ratings

Parameter	Min.	Typ.	Max.	Unit
VESD – HBM			±2000	V
VESD – CDM			±500	V

Operating Range

Operating range defines the supply voltage and temperature ranges where this device is functional.

Table 5: WA1470 Operating Range

Parameter	Min.	Typ.	Max.	Unit
Operating supply voltage (V_{BAT})	1.8	3.3	3.6	V
Operating ambient temperature range	-40	25	+85	°C

Performance Specifications

Table 6: WA1470 Performance Specifications

Specification	Min	Typ	Max	Units	Comments/Test Condition
Band of Operation					
Lower Band	430		500	MHz	
Upper Band	860		925	MHz	
Current Consumption					
Shutdown Current			5	uA	Disconnecting Crystal and forcing Enable low – All chip blocks are off
Deep Sleep Current[1]		2.5	4.5	mA	Digital Backend only is ON and the rest of chip is off
Sleep Current[1]		3.2	5.0	mA	Digital Backend and Core Bias cells are ON – Rest is off
Idle Current[1]		9	13	mA	Same as Sleep mode + Frequency Synthesizer is ON
Receiver Current[1] Upper Band		17.5	25.0	mA	Complete Rx chain is ON
Tx BPSK[1] Upper Band		50	60	mA	Complete TX Chain is ON @Max Output Power
Receiver Specifications					
S11		-11		dB	
Gain	47		92	dB	
Gain Step		3.0		dB	
NF		3.6		dB	
Input P1dB		-40		dBm	@ Rx Gain = 44 dB
IIP3		-50		dBm	@ Rx Gain = 44 dB
DC Offset (VGA Output)	±3		±20	mV	
Transmitter (BPSK mode) Specifications					
Max output Power (@ PA Gain setting = 21)	12	15	17	dBm	
Min Output Power (@ PA Gain Setting = 0)	-25	-10	-8	dBm	
Output Power Step	1.2	3.0		dB	

Maximum and Minimum are across temperature.

[1]Digital Backend is up without a specific activity which gives uncertainty in current consumption

Description of the Registers

eFuse Mirror Registers

These are the registers that can be reloaded automatically at ASIC startup from the pre-programmed eFuse every power up.

Table 7: WA1470 eFuse Mirror Registers

Addr [Hex]	Default [Bin]	Bit	Name	Description
4000	011	7:5	pll_ivco_ctrl	Trimming bias current in VCO
	01	4:3	pll_icp_ctrl	Trimming PLL-CP current
	1	2	pll_sdm_en	Enable FracN mode (SDM) of PLL
	1	1	pll_sdm_third	Enable SDM in 3rd order mode
	0	0	pll_sdm_fourth	Enable SDM in 4th order mode
4001	01	7:6	pll_vmux_sel	Control VCO control voltage if “pll_muxoverride_n”=0
	000101	5:0	pll_adccal_1v2	Control ADC calibration clock frequency
4002	0	7	txrx_bandsel	Control the RF band of the TRx 1 for 860MHz – 925MHz band 0 for 430MHz – 500MHz band
	0011	6:3	lna_ictrl	Trimming of bias current in LNA
	11	2:1	lna_gctrl	Trimming of LNA gain
	0	0	rx_mode	Not Used
4003	01	7:6	mixer_ictrl	Trimming of bias current in Rx Mixer Gm stage
	0101	5:2	mixer_tia_gctrl	Control of Rx mixer TIA gain
	1	1	rx_occ_en	Enable Rx offset cancellation
	1	0	tx_occ_en	Enable Tx offset cancellation
4004	01	7:6	sadcrefbufftrim	Trimming of ADC reference voltage
	000111	5:0	sadci_trimmingman	Trimming of I-Channel ADC delay unit
4005	0	7	sadci_adccomprstplssel	Trimming of I-Channel ADC reset pulse
	1	6	sadci_trimmingmansel	Select between auto & manual trimming of I-Channel ADC delay unit
	01	5:4	tmpsns_reftrim	Trimming of TMPSNS reference voltage
	0	3	vga_f3db_tune_override	Enable bypassing Rx LPF tuning

Addr [Hex]	Default [Bin]	Bit	Name	Description
	0	2	eFuse_fully_burned	Should be programmed as 1 to enable the ASIC auto initialization
	10	1:0	vco_cap_tune	Trimming of VCO output frequency
4006	000111	7:2	sadcq_trimmingman	Trimming of Q-Channel ADC delay unit
	1	1	sadcq_trimmingmansel	Select between auto & manual trimming of Q-Channel ADC delay unit
	0	0	txmode	1 for Tx BPSK mode 0 for Tx IQ mode
4007	0000	7:4	tx_pcalib_q_c	Coarse trimming of Tx LO signal of Q-Channel
	0000	3:0	tx_pcalib_q_f	Fine trimming of Tx LO signal of Q-Channel
4008	0	7	vga_filt_4th_to_2nd	Not Used
	0	6	rxadc_adcpsen	Enable power saving mode in Rx ADC (Not Recommended)
	0	5	rxadc_adccompensel	Controls Rx ADC comparator enable in power saving mode
	0	4	rxadc_compvalidmode	Enable auto synchronous cycling of Rx ADC
	01	3:2	tia_ictrl	Trimming of Rx Mixer TIA bias current
	0	1	mixer_cm_ctrl	Trimming CM level of Rx I-Channel mixer
	0	0	gpadc_compvalidmode	Enable auto synchronous cycling of TMPSNS ADC
4009	01010101	7:0	bctrl [7:0]	Trimming Rx VGA bias current
400A	01	7:6	bctrl [9:8]	Trimming Rx VGA bias current
	0	5	gpadc_adccomprstplssel	Trimming of TMPSNS ADC reset pulse
	1	4	gpadc_trimmingmansel	Select between auto & manual trimming of TMPSNS ADC delay unit
	0	3	tx_extpa_mode	Enable Tx with External PA mode
	0	2	txpa_ldo_byp	Enable bypass mode of PA LDO
	11	1:0	tx_cml_ibias_ctrl	Trimming bias current of Tx CML buffer in external PA mode
400B	0000	7:4	rx_pcalib_i_c	Coarse trimming of Rx LO signal of I-Channel
	0000	3:0	rx_pcalib_i_f	Fine trimming of Rx LO signal of I-Channel

Addr [Hex]	Default [Bin]	Bit	Name	Description
400C	000111	7:2	gpadc_trimmingman	Trimming of TMPSNS ADC delay unit
	0	1	gpadc_adcpsen	Enable power saving mode of TMPSNS ADC (Not Recommended)
	0	0	gpadc_adccompensel	Controls TMPSNS ADC comparator enable in power saving mode
400D	0000	7:4	vga_f3db_tune	Rx LPF tune manual control
	0000	3:0	txdac_f3db_tune	Tx LPF tune manual control
400E	1	7	clkgenrst	Reset of ADC clock generator
	0	6	clkgenen	Enable of ADC clock generator
	000000	5:0	sampleclkpw1	Trimming pulse width of Rx ADC sampling clock
400F	000000	7:2	sampleclkperiod1	Trimming frequency of Rx ADC sampling clock
	00	1:0	lna_cap_tune	Trimming frequency tuning of LNA
4010	000000	7:2	sampleclkpw2	Trimming pulse width of TMPSNS ADC sampling clock
	0	1	paldo_cc_ctrl	Enable PA LDO output compensated mode (Not Tested)
	0	0	rx_lna_ldo_mode	Enable high load current of LNA LDO (Not Tested)
4011	000000	7:2	sampleclkperiod2	Trimming frequency of Rx ADC sampling clock
	0	1	pa_mode_ext	Enable 3V PA LDO output if “pa_mode_bypass”=1
	0	0	pa_mode_bypass	Bypass internal auto control of PA LDO output voltage level
4012	000000	7:2	compenpw1	Control Rx ADC comparator enable pulse in power saving mode
	00	1:0	tx_sel_txmixer_1v2	LSB controls of TX mixer CM level
4013	000000	7:2	compenpw2	Control TMPSNS ADC comparator enable pulse in power saving mode
	0	1	rx_mixer_ldo_1p4v_ctrl	Enable 1.4V mode of Mixer LDO
	0	0	sadcq_adccomprstplssel	Trimming of Rx Q-Channel ADC reset pulse

Addr [Hex]	Default [Bin]	Bit	Name	Description
4014	0000	7:4	rx_pcalib_q_c	Coarse trimming of Rx LO signal of Q-Channel
	0000	3:0	rx_pcalib_q_f	Fine trimming of Rx LO signal of Q-Channel
4015	0000	7:4	tx_pcalib_i_c	Coarse trimming of Tx LO signal of I-Channel
	0000	3:0	tx_pcalib_i_f	Fine trimming of Tx LO signal of I-Channel
4016	000000	7:2	sclk_ndiv	Control Tx DAC sampling clock frequency
	1	1	dem_lfsr_en	Enable Tx DAC LFSR mode for DEM
	1	0	dem_cntr_en	Enable Tx DAC normal counter mode for DEM
4017	0	7	lprlxosc_en	Enable 1kHz LP RCO
	0000000	6:0	lprlxosc_ftrim	Trimming frequency of 1kHz LP RCO
4018	0	7	hprlxosc_en	Enable 20MHz RCO
	0000000	6:0	hprlxosc_ftrim	Trimming frequency of 20MHz RCO
4019	111	7:5	lpref_vtrim	Trimming LDODIG LP reference voltage
	1111	4:1	lpref_itrim	Trimming LDODIG LP reference current
	0	0	lpref_1p2en	Enable 1.2V mode of LDODIG
401A	00000000	7:0	chp_id[7:0]	Reserved for chip ID
401B	00000000	7:0	chp_id[15:8]	Reserved for chip ID
401C	00000000	7:0	chp_id[23:16]	Reserved for chip ID
401D	00000000	7:0	chp_id[31:24]	Reserved for chip ID
401E	0	7	padsmt	7Enable Schmitt trigger in digital IO pads
	0	6	pade1	Trimming drive strength of digital IO pads
	0	5	pade2	
	0	4	padpos	Power on start control of digital IO pads 0: active pull down disabled for loss of core power 1: active pull down enabled for loss of core power
	0	3	padsr	Slew rate control of digital IO pads 0: slow (half frequency) 1: fast

Addr [Hex]	Default [Bin]	Bit	Name	Description
	0	2	padp2	Disabled state control of digital IO pads [Hi-Z/Pull-up/Pull-down/Repeater]
	0	1	padp1	
	0	0	padsel18	Pad-frame control 1 for DVDD ≤ 1.8V 0 for DVDD ≥ 2.5V
401F	1		mixer_cm_ctrl_q	Trimming CM level of Rx Q mixer
	1		rx_ldo_mixer_en	Enable mixer LDO
	1		tx_sel_txmixer_1v2[2]	MSB of trimming Tx mixer CM level
	1		vcoldo_1p4enb	Enable VCO LDO 1.4V mode (active low)
	1		lnaldo_1p4enb	Enable LNA LDO 1.4V mode (active low)
	1		lckdet_mode	Define mode of auto PLL lock detection 0 for narrow range detection 0.4V–0.8V 0 for wide range detection 0.2V–1V
	1		lckdet_en	Enable auto PLL lock detection
	1		tx_vga_ictrl[1]	MSB of Tx VGA bias current trimming

Non-eFuse Writable Registers

These are the registers that can be changed by SPI write command, but they have no eFuse mirror and can't be loaded automatically at ASIC power up.

SPI write commands should be executed after power up for any change of value required in these registers.

Table 8: WA1470 Non-eFuse Writable Registers

Addr [Hex]	Default [Bin]	Bit	Name	Description
4020	00000101	7:0	eFuse_addr	eFuse bit address
4021	0	7	eFuse_ctrl_doProgByte	Enable eFuse program byte
	0	6	eFuse_ctrl_doReloadByte	Enable eFuse reload byte
	0	5	eFuse_ctrl_doProgAll	Enable eFuse program all
	0	4	eFuse_ctrl_doProg	Enable eFuse program bit
	0	3	eFuse_ctrl_doReload	Enable eFuse reload all
	0	3	eFuse_ctrl_doRead	Enable eFuse read byte
	10	1:0	eFuse_ctrl_Mode	Control mode of eFuse

Addr [Hex]	Default [Bin]	Bit	Name	Description
4022	0	7	pll_cal_add_sub	Add/Sub from VCO tuner output
	00	6:5	pll_cal_offset	Insert offset from VCO tuner output
	10000	4:0	pll_cal_tune	Manual control of VCO instead of VCO tuner
4023	100010	7:2	pll_nint	PLL integer division ratio
	00	1:0	pll_icp_offset	PLL CP offset control
4024	1	7	pll_1gdiv2mux_1gdiv2_en	Enable 1GHz post VCO divider
	1	6	pll_1gdiv2mux_en	Enable 1GHz post VCO mux
	1	5	pll_2gdiv2_en	Enable 2GHz post VCO divider
	1	4	pll_cp_en	Enable PLL CP
	1	3	pll_cp_nmirror_en	Enable PLL CP NMOS
	1	2	pll_cp_opamp1_en	Enable PLL CP 1st opamp
	1	1	pll_cp_opamp2_en	Enable PLL CP 2nd opamp
	1	0	pll_cp_pmirror_en	Enable PLL CP PMOS
4025	1	7	pll_en	Enable PLL
	1	6	pll_pfd_en	Enable PLL PFD
	1	5	pll_buffer_en	Enable PLL buffer
	1	4	pll_ldo_en	Enable PLL LDO
	1	3	pll_vco_ibias_en	Enable PLL VCO bias current
	1	2	pll_vco_en	Enable PLL VCO
	1	1	pll_vco_varactor_en	Enable PLL VCO varactor
	1	0	pll_vco_capbank_en	Enable PLL VCO capacitor bank
4026	00000000	7:0	pll_nfrac[7:0]	PLL fractional division ratio
4027	00000000	7:0	pll_nfrac[15:8]	PLL fractional division ratio
4028	0000000	7:1	pll_nfrac[22:16]	PLL fractional division ratio
	1	0	tx_mixer_en	Enable Tx mixer
4029	1000	7:4	vga1_gctrl	Control gain of 1st stage in Rx VGA
	1000	3:0	vga2_gctrl	Control gain of 2nd stage in Rx VGA
402A	011	7:5	txmixer_gctrl	Control gain of Tx CML buffer

Addr [Hex]	Default [Bin]	Bit	Name	Description
	1	4	tx_en	Enable Tx
	0	3	bb_tuner_start	Enable LPF tuner
	1	2	tx_bb_dac_en	Enable Tx DAC
	1	1	tx_bb_dac_lpf_en	Enable Tx LPF
	0	0	tx_vga_ictrl[0]	LSB of Tx VGA bias current control
402B	1	7	sadcrefbuffen	Enable ADC reference buffer
	0	6	sadcrefbuff_highz	Enable Hi-Z mode of ADC reference buffer
	1	5	sadci_adcen	Enable Rx I-Channel ADC
	0	4	Spare_wr_C_1	Not Used
	1	3	sadcq_adcen	Enable Rx Q-Channel ADC
	0	2	gpadc_adcen	Enable TMPSNS ADC
	0	1	gpadc_calbstart	Rising edge trigger of TMPSNS ADC manual Calibration
	0	0	gpadc_calbseqstart	Rising edge trigger of TMPSNS ADC auto Calibration
402C	1	7	rx_biquad_en	Enable Rx VGA
	1	6	rx_biquad_filt1_en	Enable Rx 1st LPF stage
	1	5	rx_biquad_filt2_en	Enable Rx 2nd LPF stage
	1	4	rx_ldo_en	Enable LNA LDO
	1	3	rx_lna_en	Enable LNA
	1	2	rx_mixer_en	Enable Rx Mixer
	1	1	rx_mixer_gmstage_en	Enable Rx Mixer Gm stage
	1	0	rx_mixer_tia_en	Enable Rx Mixer TIA
402D	000	7:5	txdac_gctrl	Control Tx DAC output swing
	00000	4:0	txpa_gctrl	Control Tx PA output power
402E	1	7	tx_pa_en	Enable Tx PA
	1	6	tx_bb_bias_en	Enable Tx baseband bias current
	1	5	tx_bb_dac_10b_en	Enable Tx DAC core
	1	4	tx_bb_en	Enable Tx baseband
	1	3	tx_ldopa_en	Enable PA LDO

Addr [Hex]	Default [Bin]	Bit	Name	Description
	1	2	tx_mixer_cml_opamp_en	Enable CML opamp
	1	1	tx_mixer_cml_en	Enable CML stage
	1	0	tx_mixer_dif2s_en	Enable Tx post mixer buffers
402F	1	7	txrx_poff	Enable deep sleep mode
	0	6	txrx_sleep	Enable sleep mode
	0	5	txrx_idle	Enable Idle mode
	0	4	txon_rxoff	1: Tx mode 0: Rx mode
	0	3	ana_test_mux_en	Not Used
	000	2:0	ana_test	Not Used
4030	1	7	pll_muxoverride_n	Enable VCO control voltage manual selection (active low)
	0	6	pll_sel_loop	Enable PLL closed loop
	0	5	pll_cal_start	Rising edge trigger of PLL auto tuning (VCO tuner)
	0	4	pll_cal_bp	Bypass VCO tuner
	0	3	adc_calclken	Enable ADC calibration clock
	0	2	rxadc_calbstart	Rising edge trigger for manual calibration of Rx ADCs
	1	1	rx_en	Enable Rx
	0	0	tmpsns_en	Enable TMPSNS
4031	0	7	ldodig_highz	Enable Hi-Z mode of LDODIG
	0	6	ldogp_en	Enable auxiliary LDO for TMPSNS & TMUX operation
	0	5	RXADC_CALBSEQSTART	Rising edge trigger for auto calibration of Rx ADCs
	0000	4:1	DMUX_MODE	Define DMUX mode
	0	0	DMUX_EN	Enable DMUX
4032	0000	7:4	TMUX_MODE	Define TMUX mode
	0	3	TMUX1_EN	Enable TMUX
	0	2	TMUX2_EN	Not Used

Addr [Hex]	Default [Bin]	Bit	Name	Description
	0	1	TMUX3_EN	Not Used
	0	0	TMUX4_EN	Not Used
4033	000000	7:2	Spare_wr_B_8[7:2]	Not Used
	0	1	ldomixer_byp	Bypass mixer LDO
	0	0	adc_tst_en	Enable testing mode of TMPSNS ADC

Read Only Registers

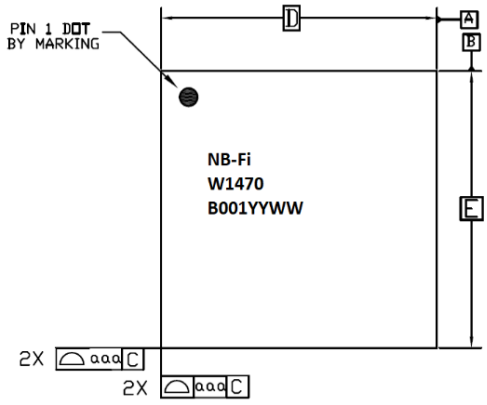
These are the registers that can ONLY be read by SPI read command and they have no eFuse mirror.

Table 9: WA1470 Read Only Registers

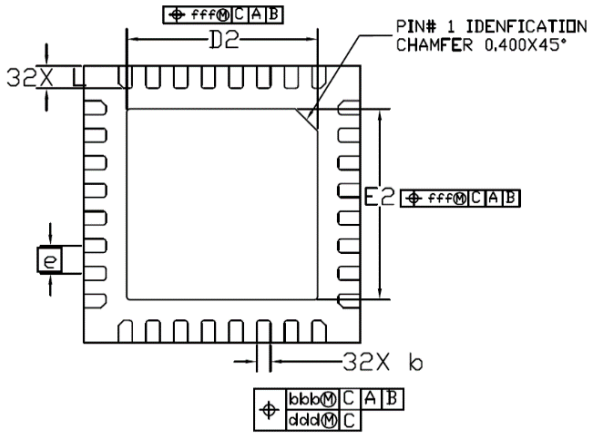
Addr [Hex]	Bit	Name	Description
4034	7:3	pll_vco_calout	VCO tuner output
	2	pll_vco_calibdone	Flag of VCO tuning operation
	1	tune_f3dB_rx_caldone	Flag of Rx LPF tuning operation
	0	tune_f3dB_tx_caldone	Flag of Tx LPF tuning operation
4035	7:4	tune_f3dB_rx	Rx LPF tuner output
	3:0	tune_f3dB_tx	Tx LPF tuner output
4036	7:0	sadci_adcout[7:0]	Output of Rx I-Channel ADC
4037	7:4	sadci_adcout[11:8]	
	3	sadci_calbdone	Flag of Rx I-Channel ADC calibration
	2	sadci_calbfailed	Flag of Rx I-Channel ADC calibration failure
	1	rxadc_calbseqdone	Flag of Rx ADCs auto calibration
	0	gpadc_calbseqdone	Flag of TMPSNS ADC auto calibration
4038	7:0	sadcq_adcout[7:0]	Output of Rx Q-Channel ADC
4039	7:4	sadcq_adcout[11:8]	
	3	sadcq_calbdone	Flag of Rx Q-Channel ADC calibration
	2	sadcq_calbfailed	Flag of Rx Q-Channel ADC calibration failure
	1	eFuse_st_cmdDone	Flag to indicate end of eFuse operation
	0	regfile_init_done	Flag to indicate ASIC initialization
403A	7:0	gpadc_adcout[7:0]	Output of TMPSNS ADC

Addr [Hex]	Bit	Name	Description
403B	7:4	gpadc_adcout[11:8]	
	3	gpadc_calbdone	Flag of Rx TMPSNS ADC calibration
	2	gpadc_calbfailed	Flag of Rx TMPSNS ADC calibration failure
	1	adc_clk_ready	Flag of PLL locking (1: PLL is locked)
	0	pmode_switch_busy	Flag to indicate ASIC modes transition is complete (0 means transition is complete)
403C	7:0	eFuse_Read_Data	eFuse read data output of read operation
403D	7:2	gpadc_trimmingcalb	Output of TMPSNS ADC calibration
	1:0	spare_rd_B_2	Not Used
403E	7:2	sadcq_trimmingcalb	Output of Rx Q-Channel ADC calibration
	1:0	spare_rd_C_2	Not Used
403F	7:2	sadci_trimmingcalb	Output of Rx I-Channel ADC calibration
	1:0	spare_rd_D_2	Not Used

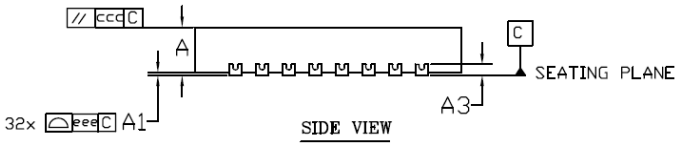
Packaging Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NF-Fi:	Name of the communication standard
W1470:	Part number
B001YYWW:	B0 – Chip version, 01 – Package Version, YYWW – Date of assembly in the form of Year, Week Number.

Dimenslonal Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
	0.700	0.750	0.800
A1	0.000	—	0.050
A3	0.203 REF		
D	5.000 BSC		
E	5.000 BSC		
D2	3.400	3.450	3.500
E2	3.400	3.450	3.500
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

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